



PATENT ABSTRACTS OF JAPAN

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ISHIKIRIYAMA MAMORU****(54) DIELECTRIC ISOLATION SUBSTRATE AND
SEMICONDUCTOR INTEGRATED CIRCUIT
DEVICE USING THE SAME****(57) Abstract:**

PROBLEM TO BE SOLVED: To aim at substantial reduction of wafer warpage amount in step with a heating process such as oxidation, diffusion, or the like by a method, wherein there is formed an oxidation-resistant film on an isolation region where a polycrystalline silicon layer on the side of a main surface of a dielectric isolation substrate is exposed, and the oxidation-resistant film of the same patterns as that of the side of the main surface is also formed on the side of the rear face.

SOLUTION: On an isolation region 100 where a polycrystalline silicon layer 103 on the side of a main surface of a dielectric isolation substrate is exposed, a first nitride film 105 as an oxidation-resistant film is formed by the use of CVD, photolithography, and an etching technique. Furthermore, a second nitride film 106 is also formed in the same manner as on the main surface on the side of the rear face of a dielectric isolation substrate. At this time, the second nitride film 106 is prepared with the same patterns as in the first nitride film 105. A semiconductor element is formed on single crystal silicon islands

101a, 101b and 101c. Thereby, it is possible to substantially reduce wafer warpage amount in a heating step, such as oxidation, diffusion, or the like. Furthermore, it is possible to eliminate the need for optimizing patterns in an oxidation-resistant film on the side of the rear face with respect to different oxidation, diffusion process conditions.

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